REMARKS

This response accompanies a Request for Continued Examination. Claims 1, 19, 24, 30, 33, 38 and 44 are currently amended. Support for all of the claims pending in the application can be found throughout pages 261 to 293 (IX. COVERIFICATION SYSTEM) of the specification and the accompanying figures. As such, no new matter has been added. In view of the above amendments and arguments below, Applicants believe that all claims are allowable.

I. REPSONSE TO ADVISORY ACTION MAILED MAY 1, 2006

The Examiner in an Advisory Action mailed May 1, 2006 maintained rejection of all claims currently pending in the application under 35 U.S.C. §102(b) and 35 U.S.C. §103(a). The Examiner states the broadest interpretation of the pending claim can be communication messages "from" (first information) and "to" (second information) software-hardware models. The Examiner further states a shared buffer (memory) on the communications channel is a "shared memory for holding a software model and a hardware model".

Applicants have amended claims 1, 19, 24, 30, 33, 38 and 44. Applicants submit the amended claims to more clearly define the invention and overcome the broadest interpretation of a "shared memory" as offered by the Examiner. These arguments are discussed in greater detail below.

II. 35 U.S.C. §102 REJECTION OF CLAIMS 1, 19, 24, 30, 33, 38 and 40

Claims 1, 19, 24, 30, 33, 38 and 40 stand rejected as being anticipated by United States Patent No. 5,663,900 issued Sep. 2, 1997 to *Bhandari et al.* (hereinafter referred to as "*BH'900*").

Applicants have amended independent claim 1 to specifically recite:

> An electronic design automation system for verifying a user design, comprising:
>
> a computing system including a central processing unit for modeling the user design in software;
>
> an internal bus system coupled to the computing system;
>
> reconfigurable hardware logic coupled to the

> internal bus system and for generating a hardware model which includes at least a portion of the user design modeled in hardware;
>
> control logic coupled to the internal bus system for controlling the delivery of data between the reconfigurable hardware logic and the computing system; and
>
> shared memory for holding a first information of a software model and a second information of the hardware model, where the second information comprises at least one internal state of the hardware model and the software model is capable of directly accessing the second information of the hardware model.
>
> (emphasis added)

Claims 19, 24, 30, 33, and 38 have been amended to recite similar limitations. *BH'900* is totally devoid of any teaching of a software model capable of directly accessing an internal state of a hardware model. By using shared memory, the internal states of the hardware model are continuously available to the software model. By making these internal states continuously available the present invention provides the advantage of allowing a user to sample different outputs of the hardware model without recompiling the design in the emulator, allows for more efficient debugging of the hardware design, and decreases setup and testing time because rewiring of the hardware model to different pin outputs is not necessary. The process of recompiling, debugging, rewiring or altering the hardware model so that an internal state is made available (converted to an external state) via a pin output is a task may take days or weeks when utilizing a conventional emulator such as shown in *BH'900*. Such a delay using a conventional emulator is often unacceptable for a time-sensitive design/development schedule. *Since BH'900* does not teach every element of Applicant's invention, specifically making an internal state available to of a hardware model available to a software model, *BH'900* does not anticipate claims 1, 19, 24, 30, 33, and 38.

In contrast, *BH'900* teaches a simulator (software model) (col. 3, 35-40) communicates with external systems (hardware model) (col. 3, lines 55-60) via interface hardware and software. (col. 3, lines 20-30). "In this configuration, an interface tool according to the present invention enables simulator 16 to co-operate or functionally interact with various external systems 45 coupled thereto." (col. 4, lines 4-6) The communication between simulator and the external system is only via

an interface and not direct access. Further, the simulator (software model) is capable of only receiving information communicated via pin outputs of the external systems (hardware model). (col. 3, lines 21-29) The simulator is incapable of directly accessing an internal state of the external system, i.e., a state of the external system not available via pin output. *BH'900* does not teach a software model capable of directly accessing an internal state of a hardware model.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added). Therefore, Applicants contend that claims 1, 19, 24, 30, 33, 38, and 44 are patentable over *BH'900* and, as such, fully satisfy the requirements of 35 U.S.C. §102 and are patentable thereunder.

Furthermore, claims 2-6, 20-23, 25-29, 31-36, and 45-46 depend, either directly or indirectly, from claims 1, 19, 24 30, 33, 38, and 44 and recite additional features therefor. Since *BH'900* does not teach Applicants' invention as recited in claims 1, 19, 30, 33, 38, and 44, dependent claims 2-6, 20-23, 27-28, 34-36, and 45 are also patentable over *BH'900*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

III. 35 U.S.C. §103(a) REJECTION OF CLAIMS 7 and 10

Claims 7 and 10 stand rejected as being unpatentable over *BH'900* in view of an article "Q-Modules: Internally Clocked Delay-Insensitive Modules" by Rosenberger et al. (IEEE Transactions on Computers, vol. 37, No. 9, Sep. 1988, pp. 1005-1018, hereinafter referred to as "*RO'1988*"). The applicants respectfully traverse the rejection.

The Examiner contends that *BH'900* teaches all the limitations of claims 7 and 10 except the timing logic. The Examiner cites *RO'1988* as teaching timing logic. The Examiner concludes that a combination of *BH'900* and *RO'1988* teach the subject matter of claims 7 and 10. The applicants respectfully disagree.

As discussed above, *BH'900* does not teach a software model capable of directly accessing an internal state of a hardware model using a shared memory as recited in claim 1 from which claims 7 and 10 depend. *RO'1988* teaches Q-modules without any teaching or suggestion of using shared memory for holding a first

information of a software model and a second information of the hardware model, where the second information comprises at least one internal state of the hardware model and the software model is capable of directly accessing the secong information of the hardware model. Since neither the *BH'900* nor *RO'1988* teach a software model capable of directly accessing an internal state of a hardware model, no combination of these references can teach a software model capable of directly accessing an internal state of a hardware model. Consequently, an element of the base claim (claim 1) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claims (claims 7 and 10) that depend from claim 1 are not taught or suggested by the cited references.

Thus, the applicants submit that claims 7 and 10 are patentable over *BH'900* in view of *RO'1988*. Accordingly, the applicants respectfully request the rejection be withdrawn.

IV. 35 U.S.C. §103(a) REJECTION OF CLAIMS 8-9 and 11-18

Claims 8-9 and 11-18 stand rejected as being unpatentable over *BH'900* in view of *RO'1988* and further view of an article "High Speed External Asynchronous/Internally clocked Systems" by VanScheik et al. (IEEE Transactions on Computers, vol. 46, No. 7, Jul. 1997, pp. 824-829, hereinafter referred to as "*VA'1997*").

The Examiner contends that *BH'900* teaches all the limitations of claims 8-9 and 11-18 except the timing logic having a first logic, second logic and third logic. The Examiner cites *RO'1988* as teaching timing logic, but the Examiner concedes that RO'1988 does not teach the first, second and third logic. As such, the Examiner cites *VA '1997* as teaching first logic, second logic and third logic. The Examiner concludes that a combination of *BH'900*, *RO'1988* and *VA'1997* teach the subject matter of claims 8-9 and 11-18. The applicants respectfully disagree.

As discussed above, *BH'900* does not teach a software model capable of directly accessing an internal state of a hardware model using a shared memory as recited in claim 1 from which claims 8-9 and 11-18 depend. *RO'1988* teaches Q-modules without any teaching or suggestion of using shared memory for holding a first information of a software model and a second information of the hardware model, where the second information comprises at least one internal state of the

hardware model and the software model is capable of directly accessing the second information of the hardware model and VA'1997 teaches delay insensitive logic modules. Since neither the *BH'900, RO'1988* nor *VA'1997* teach a software model capable of directly accessing an internal state of a hardware model, no combination of these references can teach a software model capable of directly accessing an internal state of a hardware model. Consequently, an element of the base claim (claim 1) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claims (claims 8-9 and 11-18) that depend from claim 1 are not taught or suggested by the cited references.

Furthermore, claims 8-9 and 11-18 depend, either directly or indirectly, from claim 1 and recite additional features therefor. Since the combination of *BH'900, RO'1988* and *VA'1997* does not teach or suggest the applicants' invention as recited in claim 1, dependent claims 8-9 and 11-18 are also not obvious and are allowable.

Thus, the applicants submit that claims 8-9 and 11-18 are patentable over *BH'900* in view of *RO'1988* and *VA'1997*. Accordingly, the applicants respectfully request the rejection be withdrawn.

V. 35 U.S.C. §103(a) REJECTION OF CLAIM 37

Claim 37 stands rejected as being unpatentable over *BH'900* in view of United States Patent No. 5,661,662 issued Sep. 2, 1997 to *Butts et al.* (hereinafter referred to as "*BU'662*").

The Examiner contends that *BH'900* in view of *BU'662* teaches all the limitations of claim 37 except "a plurality of field programmable logic devices couple together separable by at most two interconnections." The Examiner cites *BU'662* as teaching such programmable logic devices. The Examiner concludes that a combination of *BH'900* and *BU'662* teach the subject matter of claim 37. The applicants respectfully disagree.

As discussed above, *BH'900* does not teach a software model capable of directly accessing an internal state of a hardware model as recited in claim 33 from which claim 37 depends. *BU'662* teaches interconnected FPGAs without any teaching or suggestion of using shared memory for holding a first information of a software model and a second information of the hardware model, where the second information comprises at least one internal state of the hardware model and the

software model is capable of directly accessing the second information of the hardware model. Since neither the *BH'900* nor *BU'662* contain a software model capable of directly accessing an internal state of a hardware model, no combination of these references can teach a software model capable of directly accessing an internal state of a hardware model. Consequently, an element of the base claim (claim 33) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claim (claim 37) that depends from claim 33 are not taught or suggested by the cited references.

Therefore, the applicants submit that claim 37 is patentable over *BH'900* in view of *BU'662*. Accordingly, the applicants respectfully request the rejection be withdrawn.

VI. 35 U.S.C. §103(a) REJECTION OF CLAIMS 39-43 AND 47-50

Claims 39-43 and 47-50 stand rejected as being unpatentable over *BH'900* in view of an article "A Heterogeneous Environment for Hardware/Software Cosimulation" by Bishop et al. (IEEE Transactions on Computers, 1997, pp. 14-22, hereinafter referred to as "*BI'1997*").

The Examiner contends that *BH'900* teaches all the limitations of claims 38 and 44, except a plurality of field programmable devices as recited in the dependent claims. The Examiner cites *BI'1997* as teaching such devices as well as other limitations of claims 39-43 and 47-50. The Examiner concludes that a combination of *BH'900* and *BI'1997* teach the subject matter of claims 39-43 and 47-50. The applicants respectfully disagree.

As discussed above, *BH'900* does not teach a software model capable of directly accessing an internal state of a hardware model as recited in independent claims 38 and 44 from which claims 39-43 and 47-50 depend. *BI'1997* teaches hardware/software co-simulation without any teaching or suggestion of using shared memory for holding a first information of a software model and a second information of the hardware model, where the second information comprises at least one internal state of the hardware model and the software model is capable of directly accessing the second information of the hardware model. Since neither the *BH'900* nor *BI'1997* teach a software model capable of directly accessing an internal state of a hardware model, no combination of these references can teach a software model

capable of directly accessing an internal state of a hardware model. Consequently, an element of the base claim (claim 33) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claims (claims 39-43 and 47-50) that depend from claims 38 and 44 are not taught or suggested by the cited references.

Therefore, the applicants submit that claims 39-43 and 47-50 are patentable over *BH'900* in view of *BI'1997*. Accordingly, the applicants respectfully request the rejection be withdrawn.

CONCLUSION

Thus, the applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Raymond R. Moser, Jr. at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

5-15-06

Respectfully submitted,

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